

6850
 CR6/CR5
 102H
 002L

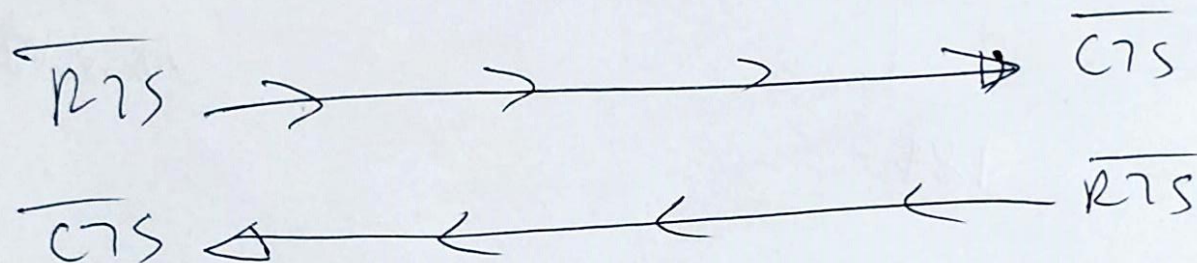
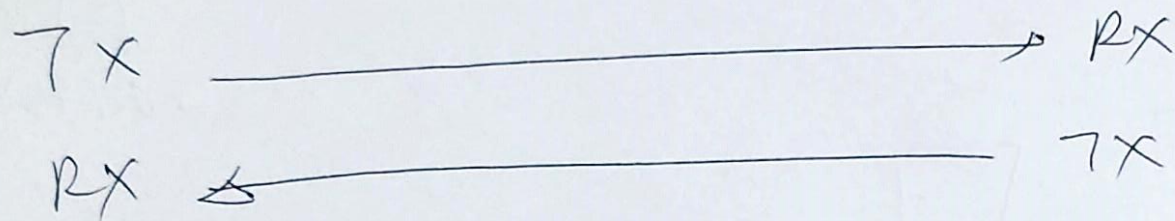
TABLE 1 — DEFINITION OF ACIA REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • R/W Transmit Data Register	RS • R/W Receive Data Register	RS • R/W Control Register	RS • R/W Status Register
	(Write Only)	(Read Only)	(Write Only)	(Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{\text{DCD}}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear to Send (CTS)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request (IRQ)

* Leading bit = LSB = Bit 0

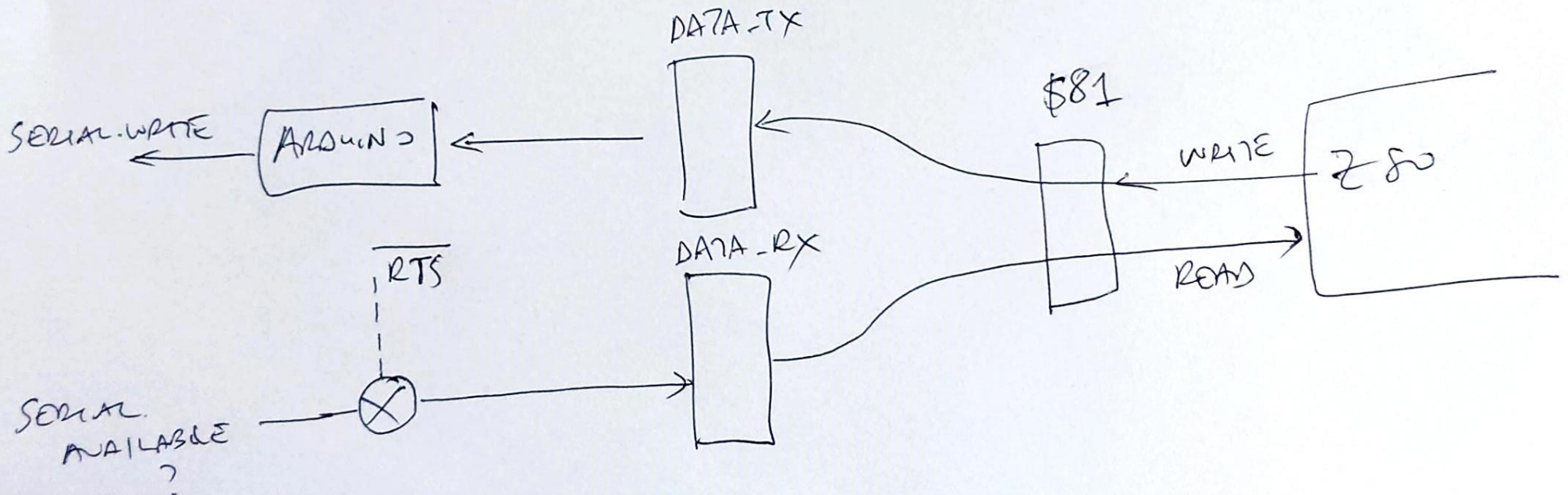
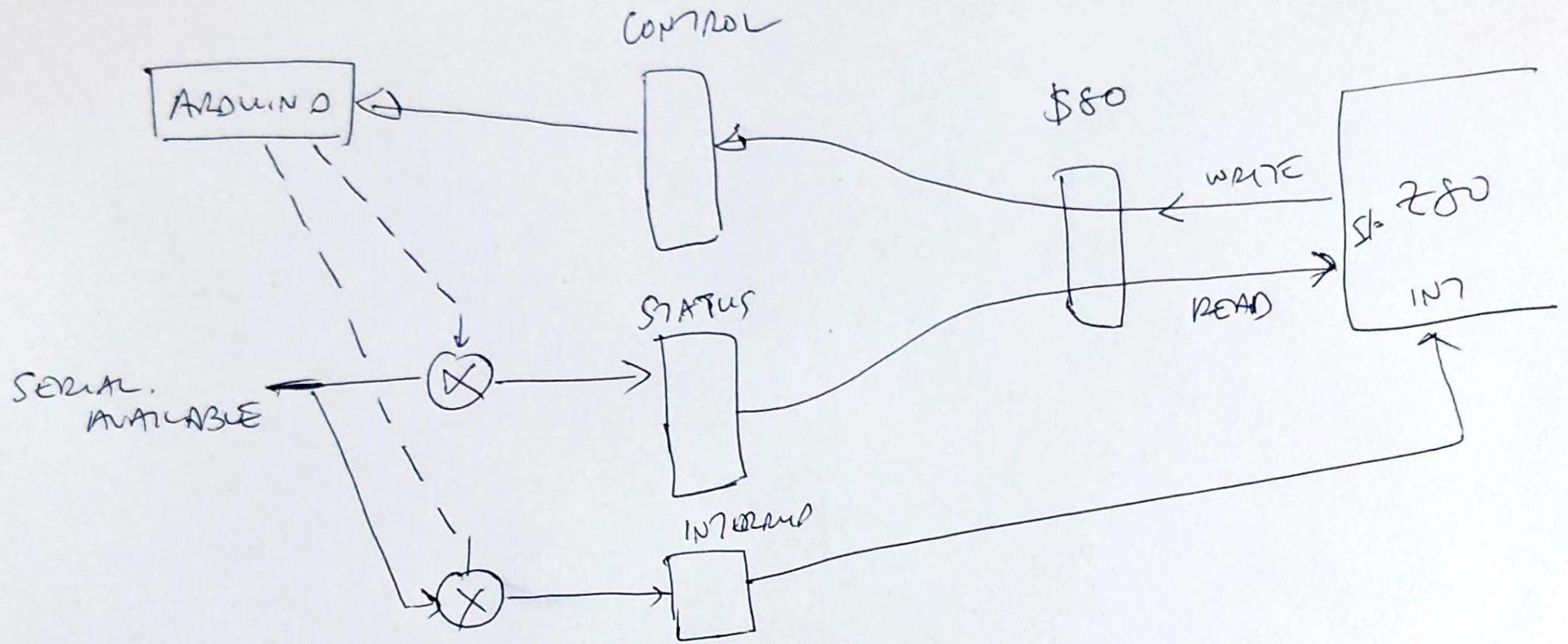
** Data bit will be zero in 7 bit plus parity modes

*** Data bit is "don't care" in 7-bit plus parity modes

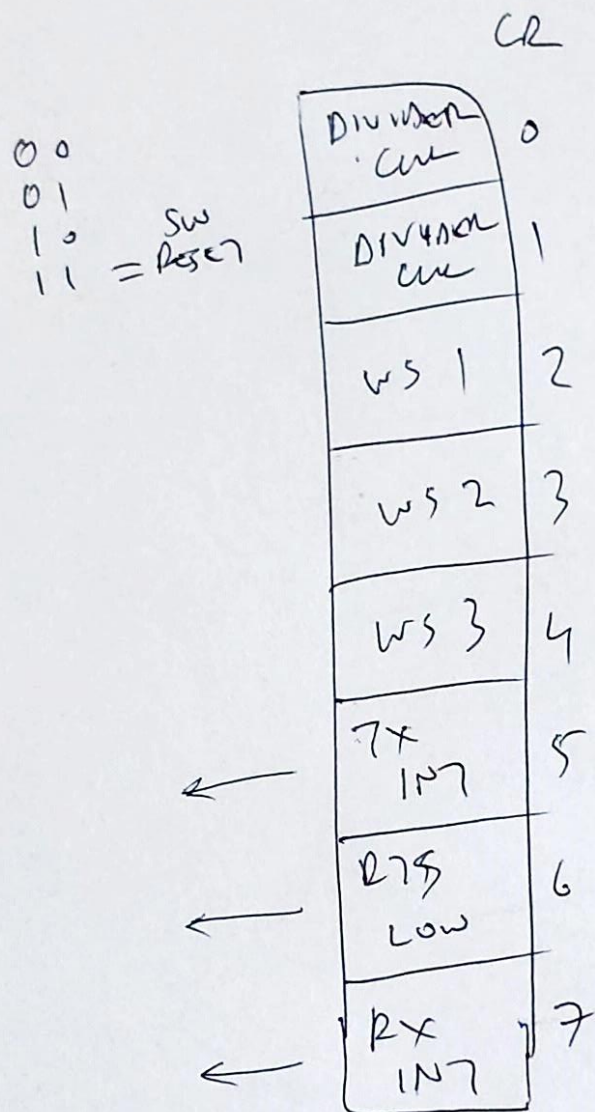


$\text{RTS} = \text{low} \Rightarrow$ You CAN SEND DATA TO ME. (CLEAR TO SEND)

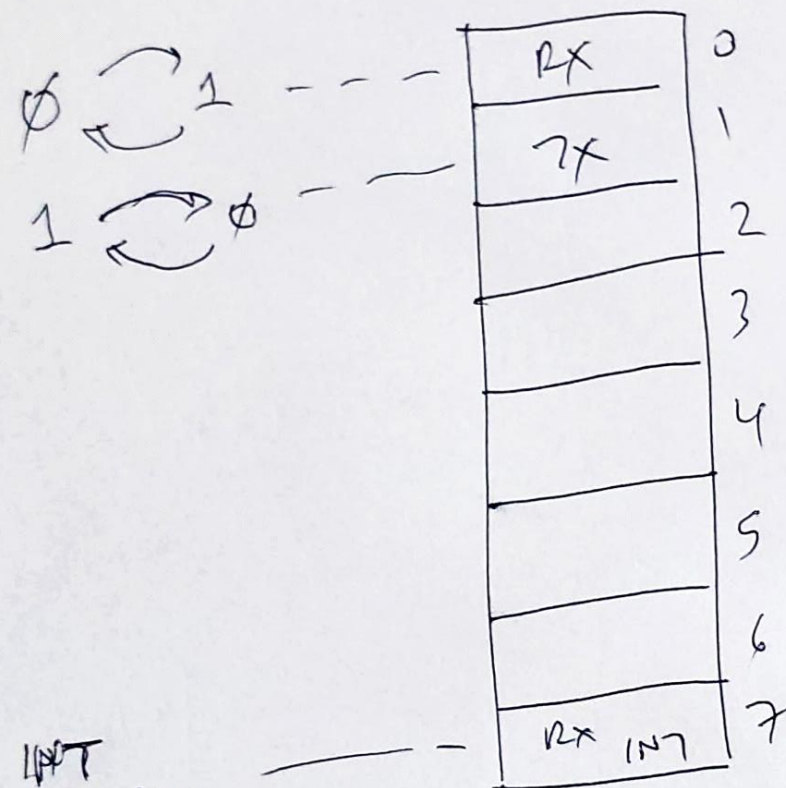
$\text{RTS} = \text{HIGH} \Rightarrow$ STOP SENDING.



CONTROL



STATUS



INT
output
from 6850

(WHY USED?)